Electronic Version
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Claims

[c1] 1.A method for forming a semiconductor device, the method comprising:
forming a first locally doped semiconductor region of a first conductivity type and a second locally doped semiconductor region of a second conductivity type over an undoped, lower semiconductor region;
implementing a first etch to simultaneously create a desired pattern in said first and second locally doped semiconductor regions in a manner that also provides a first passivation of exposed sidewalls of said first and second locally doped semiconductor regions, wherein said first etch removes material from said first and second locally doped semiconductor regions at a substantially constant rate with respect to one another, and in a substantially anisotropic manner; and
implementing a second etch to complete said desired pattern in said undoped, lower semiconductor region in a manner that protects said first and second locally doped semiconductor regions from additional material removal therefrom.

[c2] 2.The method of claim 1, further comprising annealing

the device so as to diffuse dopant from said first and second locally doped semiconductor regions into respective patterned lower semiconductor regions thereof.

[c3] 3.The method of claim 1, wherein said first etch is implemented using a patterned hardmask layer and a patterned photoresist layer over said first and second locally doped semiconductor regions.

[c4] 4.The method of claim 3, wherein said first etch is implemented using a fluorine based plasma chemistry.

[c5] 5.The method of claim 4, wherein said photoresist layer includes a carbon containing species.

[c6] 6.The method of claim 5, wherein said first passivation includes a fluorocarbon based polymer.

[c7] 7.The method of claim 3, further comprising removing said patterned photoresist layer and said first passivation following said first etch, wherein the removal of said photoresist layer and said first passivation further results in the formation of a second passivation of exposed sidewalls of said first and second locally doped semiconductor regions.

[c8] 8.The method of claim 7, wherein said second passivation protects said first and second locally doped semi-

conductor regions from additional material removal therefrom during said second etch.

[c9] 9.The method of claim 8, wherein said patterned photoresist layer and said first passivation are removed with an oxygen based plasma, and wherein said second passivation further comprises an oxide layer.

[c10] 10.The method of claim 4, wherein said first etch comprises at least one of an NF_3/Ar, a CF_4/SF_6 and a CF_4/NF_3 etch chemistry.

[c11] 11.A method for forming a semiconductor device, the method comprising:
forming a locally doped N-type polysilicon region and a locally doped P-type polysilicon region over an undoped, lower polysilicon region;
implementing a first etch to simultaneously create a gate conductor pattern in said locally doped N-type and P-type polysilicon regions in a manner that also provides a first passivation of exposed sidewalls of said locally doped N-type and P-type polysilicon regions, wherein said first etch removes material from said locally doped N-type and P-type polysilicon regions at a substantially constant rate with respect to one another, and in a substantially anisotropic manner; and
implementing a second etch to complete said gate con-

ductor pattern in said undoped, lower polysilicon region in a manner that protects said locally doped N-type and P-type polysilicon regions from additional material removal therefrom.

[c12] 12.The method of claim 11, further comprising annealing the device so as to diffuse dopant from said locally doped N-type and P-type semiconductor regions into respective patterned lower polysilicon regions thereof.

[c13] 13.The method of claim 11, wherein said first etch is implemented using a patterned hardmask layer and a patterned photoresist layer over said locally doped N-type and P-type polysilicon regions.

[c14] 14.The method of claim 13, wherein said first etch is implemented using a fluorine based plasma chemistry.

[c15] 15.The method of claim 14, wherein said photoresist layer includes a carbon containing species.

[c16] 16.The method of claim 15, wherein said first passivation includes a fluorocarbon based polymer.

[c17] 17.The method of claim 13, further comprising removing said patterned photoresist layer and said first passivation following said first etch, wherein the removal of said photoresist layer and said first passivation further results

in the formation of a second passivation of exposed sidewalls of said locally doped N-type and P-type polysilicon regions.

[c18] 18.The method of claim 17, wherein said second passivation protects said locally doped N-type and P-type polysilicon regions from additional material removal therefrom during said second etch.

[c19] 19.The method of claim 18, wherein said patterned photoresist layer and said first passivation are removed with an oxygen based plasma, and wherein said second passivation further comprises an oxide layer.

[c20] 20.The method of claim 14, wherein said first etch comprises at least one of an NF_3/Ar, a CF_4/SF_6 and a CF_4/NF_3 etch chemistry.